Texas Instruments

What a Designer Should Know

Application Report

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What a Designer Should Know

During the development of systems using integrated circuits, the engineer is frequently confronted with questions which are only partially - if at all - answered by information in data sheets, which usually give information on behavior only under recommended operating conditions. However, information is frequently needed regarding the behavior of the component outside the conditions in the data sheet. The question might be how a bus driver behaves with reduced (or even switched-off) supply voltage; or how the delay time of a gate with a large capacitive load changes; or what must be considered when using so-called "backdriving".

This report is intended to give information on a number of questions which experience has shown frequently arise. In addition, it uses examples to explain phenomena which the designer should be aware of, in order to avoid any unpleasant surprises when integrated circuits are used outside their recommended operating conditions.

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1. Introduction

The function and behavior of digital integrated circuits are fully described in data sheets. With the information given, most of the questions regarding the behavior of the component which arise when developing a system can be answered. However, in individual cases the circuits may be operated under conditions not covered by the data sheet. This report is intended to address this problem, and to give the development engineer information regarding the behavior of IC's under such conditions.

Much of the data given here is not measured when the circuits are tested; it is based on typical values which have been established experimentally, and which are applicable to the majority of components of the same type or family. The user must therefore accept that in individual cases he may need to make his own interpretation of the data, and possibly make his own measurements, in order to be able to make a sufficiently accurate forecast of the behavior of the complete system.

2. Behavior with reduced supply voltage

Although not specifically mentioned on data sheets, integrated circuits contain a number of additional components, some of them parasitic; these can influence the function of a system if the circuits are not operated within their recommended operating conditions. For example, large systems often have the requirement that parts of the system can be shut down, whilst others continue to operate. Problems most frequently occur at the interfaces between subsystems, which are now operated with different supply voltages, or whose supply is switched off completely. In this section the behavior of digital circuits when operated with low supply voltages will be described.

2.1. Behavior with switched-off supply voltage

Because of the many kinds of circuits which may be used with the various logic families, it is not possible to give any generalized rule. For this reason, only the most important circuits and their behavior will be discussed.

2.1.1. Bipolar circuits

Fig 1 shows the simplified circuit of a TTL component having diode inputs, such as are used for example with circuits in the logic family SN74LS. The following comments can however be applied to all other bipolar logic families.

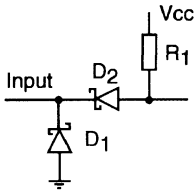

Figure 1: Input circuit of a bipolar IC

If the supply voltage in a system is switched off (V_{CC} = 0 V), then one can usually assume that the V_{CC} pin of an IC is short-circuited to ground via the other components in the system. If now a voltage is applied to the input of an IC as shown in Fig 1, and if this voltage lies within the usual logic level range (Vi = 0 ... 5.5 V), then the diode D_2 will be blocking. The clamping diode D_1 is also biased into a blocking state. A very small current therefore flows into the IC, corresponding to the leakage current of these diodes: as a value for this, the one given in the data sheets for the corresponding input voltage can be used. This statement can be applied without exception to all TTL IC's.

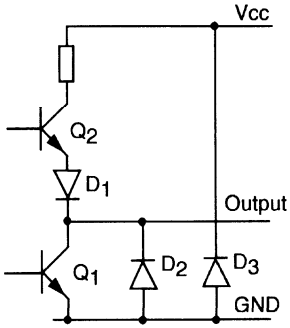

Figure 2: Output of ICs from the family SN74 (Standard TTL)

Because of the very many circuit variations that are used with the various bipolar families, the outputs of the components show a very diverse behavior. Fig 2 shows the output stage of circuits from the series SN74 (Standard TTL). Indicated are the parasitic diodes such as the collector-substrate diode D_2, and a further diode D_3, which exists in a blocking direction between the V_{CC} and GND potential connections of all integrated circuits. If the V_{CC} pin is at GND potential and a positive voltage is applied to the output, then the diode D_1 will be blocking and the output will be at a high impedance.

Other relationships result when applied to Schottky TTL circuits (Series SN74LS, SN74S, SN74ALS, SN74AS, SN74F). Fig 3 shows the most important parts of the output stage. If a voltage is applied to the output of such a circuit, whose supply

voltage is switched off, then the parasitic diode D_1 which is in parallel with the resistor R will become conducting: the output will then be at a low impedance.

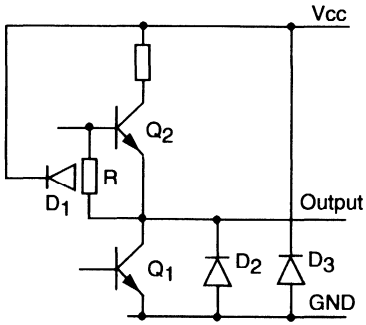

Figure 3: Output of Schottky TTL ICs

The layout of the previously shown circuit has been modified for bipolar circuits having 3-state outputs, since the parasitic diode D_1 at the output is no longer significant. One of the various possibilities here is to tie the resistor R to GND potential and not to the output of the circuit - Fig 4. In this case, the output remains at a high impedance when the supply voltage is switched off.

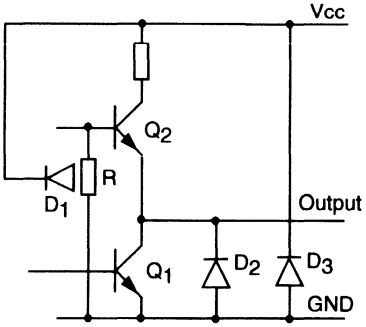

Figure 4: 3-State output of Schottky TTL Circuits

The outputs of TTL circuits with an open collector are always at a high impedance when the supply voltage is switched off.

2.1.2. CMOS circuits

The behavior of CMOS circuits when the supply voltage is switched off is essentially determined by the protective circuits at the inputs and outputs; these are intended to protect the component from damage as a result of electrostatic discharge. Fig 5

shows in simplified form the construction of a CMOS circuit with additional diode paths at input and output. It will be seen that both the input via the diode D_1, and the output via the diode D_3, are at low impedance when the supply voltage is switched off. The diode D_3 also exists with circuits having an open drain at the output.

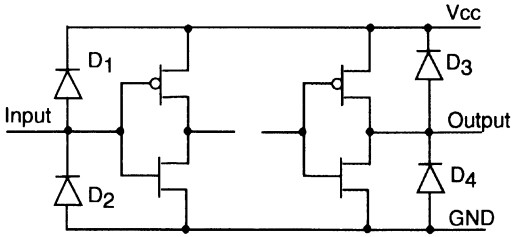

Figure 5: Diode paths in CMOS circuits

2.2. Behavior with low supply voltages

The behavior of integrated circuits at low supply voltages can be predicted only with difficulty, since in this case a detailed knowledge of the internal circuit, including its dimensions, is necessary. Using as an example the non-inverting buffer with open collector output SN7407, the behavior when switching the supply voltage on and off will now be examined. Fig 6 shows the internal circuit of the SN7407. At supply voltages lower than the forward voltage of the diode path (base-emitter path), all transistors are blocking. The output voltage V_O therefore at first follows the supply voltage V_{CC}. When the latter reaches a value of about 0.7 V, a current will flow via the resistor R_3 into the base of the transistor Q_4, such that the output switches to a Low level. If the supply voltage continues to rise and reaches a value of 3 x V_{be}, and if a logic High is applied to the input, then a current will flow into the base of transistor Q_3 (via transistors Q_1 and Q_2) which will cause it to switch. In this way the output transistor Q_4 will again be switched off, causing the output voltage to rise to a value of V_{CC}. In the previous analysis, the fact that a certain voltage drop is necessary across the resistors, in order that a sufficient base current is reached to switch on the transistor, has been neglected. It has been found in practice that TTL circuits attain stability with a supply voltage of about 3.5 V, and at a typical voltage of 4 V are fully functional. It must however be remembered that, with supply voltages below the minimum specified in data sheets, not all parameters can be guaranteed. This applies to both DC parameters such output currents and voltages, and also to AC parameters such as propagation delay time and maximum clock frequency.

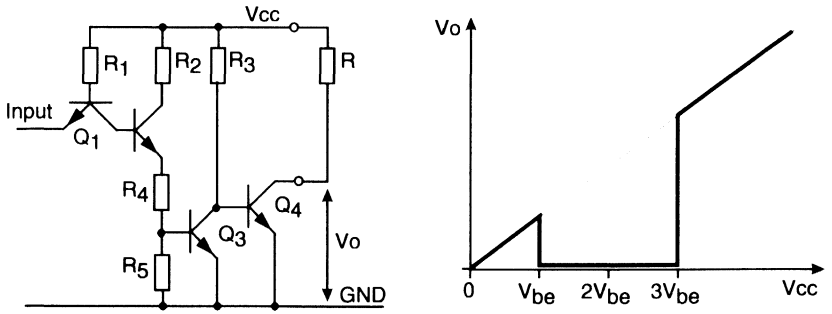

Figure 6: Behavior of a TTL circuit at low supply voltages

In a similar way to TTL circuits, CMOS circuits also fail to operate at supply voltages below the threshold voltages of the MOS transistors. If the supply voltage is further increased, parts of the circuit will be activated, as shown in Fig 6. No statement can, however, be made at this stage as to the behavior of the circuit, because as previously mentioned the precise circuit configuration of the component will be decisive. Full functionality of CMOS circuits from the family SN74HC is guaranteed from $V_{CC} = 2$ V, whereas the family 74AC can only be guaranteed from 3 V - although the latter also are stable with a supply voltage of only 2 V. In this connection it should be noted that the maximum clock frequency of CMOS circuits is dependent on the supply voltage. This can have the result that, when used at a high clock frequency, circuits do not operate reliably during the switch-on or -off phases, even though the supply voltage is more than 2 V.

An exception to this is a range of circuits with which, as a result of a special design, measures have been taken such that a defined behavior is achieved, even when they are operated at supply voltages far below the conditions recommended in data sheets. As examples, the bus drivers of the BiCMOS series SN74ABT/BCT may be mentioned. With these, a voltage monitoring circuit ensures that the 3-state outputs remain in a high impedance state at supply voltages below about 3.5 V, regardless of the signals which are applied to the inputs of these circuits. At supply voltages above this threshold voltage the control inputs (Enable, Disable) are effective: if a voltage level is applied to these inputs which results in a high impedance at the output, then this same state will be implemented at the output.

2.3. Partial switch-off of supply voltages

In large systems it often happens that part of the voltage supply is switched off, whilst other parts of the system continue to operate. The critical part of the circuit is then the interface between that which is, and that which is not, supplied with voltage. In such a case two requirements must be met. On the one hand, the part of the circuit which continues to operate must not be disturbed by the part which is switched off; on the other hand, the switched-off part must not be disturbed by fed-back voltages from the operating part.

These requirements can be met without any great difficulty with bipolar circuits. As previously mentioned, the inputs of switched-off bipolar circuits are at a high impedance, so that they will not influence parts of the circuit which are still active. With the outputs of parts of circuits which are switched off, which are connected to active circuits, it must be remembered that only the outputs of bus drivers (e.g. SN74xx240 or SN74xx245) are at a high impedance. Therefore, only such circuits should be used for bus lines connecting systems. For unidirectional lines, which connect switched-off and active circuits, a decision must be made in each individual case, whether the operation of the system could be influenced by the outputs being at a low impedance when switched off. If this is not the case, then at this position in the system any kind of circuit (including CMOS) can be used.

In addition it should be noted that, as previously mentioned, when switching the supply on and off, the logic state of the circuits concerned can not be guaranteed. This means that undefined states can arise during this time at the interfaces, which can put in question the function of the system (see Fig 6). In such a case, the use of bus drivers from the series SN74ABT/BCT will provide a solution, since the outputs of these circuits go into a high-impedance, inactive state at supply voltages below about 3.5 V.

A difficult and sometimes insoluble situation arises in the above case when using CMOS circuits. As already shown in Fig 5, these components have protection diodes at both inputs and outputs, which are connected to the supply rails. If now the supply voltage V_{CC2} of this circuit is switched off (Fig 7) whilst the supply voltage V_{CC1} remains switched on, then a current I will flow out of the gate G_1 via the diode D_1 into the next circuit, which can very rapidly overload the protective diode D_1 (the maximum current of the input clamp diodes of CMOS circuits is only 20 mA), and so destroy the circuit. Here it must be remembered that in general the next circuit represents a short circuit, so that - apart from the output resistance of the gate G_1 - there is no current-limiting circuit element.

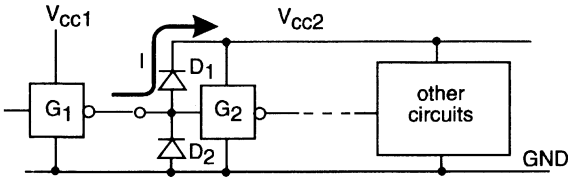

Figure 7: Feeding back with CMOS circuits

In order to avoid this situation, various circuit design ideas are to be found in the literature, but these can only be recommended with some reservations (Fig 8). In Fig 8a, the input current of the switched-off circuit is limited with resistor R. In this way the input current of the circuit to be protected can be limited to a permissible value; since the input current of CMOS circuits is extremely low, series resistors of several kiloohms usually have no negative effect on the function of the circuit. However, feeding of the next circuit via the input clamping diode D_1 will not be entirely prevented.

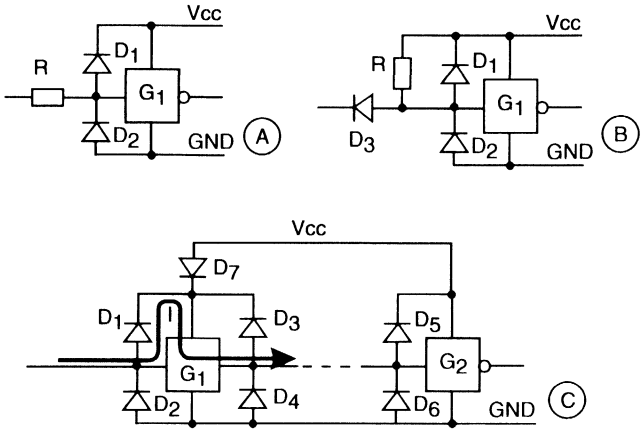

Figure 8: Circuit ideas for protecting CMOS circuits

In the circuit variant of Fig 8b, the flow of current into the circuit to be protected when the supply voltage V_{CC} is switched off is prevented with the diode D_3. However, in order to ensure a High level at the input of gate G_1 with normal operation, the "pull up" resistor is needed, and this increases significantly the power consumption of the CMOS system. It must also be noted that the diode D_3 shifts the logic level at the input of the gate, and as a result reduces the noise margin of the circuit. Apart from the latter restriction, this circuit variant is somewhat complicated, yet effective, since it really prevents feedback into the switched-off part of the circuit.

The diode in Fig 8c has absolutely no effect if the circuit G_1 has a non-inverting function. It is certainly true that as a result of it, the flow of a current via the clamping diode D_1 and the V_{CC} rail of the circuit G_1 into the next circuit is prevented. Instead of this, the current flows via the output of the gate G_1 (which in this case is at a High logic level) and so into the following circuit.

2.4. Changing subsystems whilst powered up

In many applications there exists the requirement that, in order to carry out service or repair work while in operation, it must be possible to change individual subsystems. Because of the phenomena described above, this is only permissible when circuit design modifications are made which, on the one hand prevent the destruction of semiconductor components, and on the other hand ensure that the operation of the rest of the system will not be disturbed.

It has been shown above that in the input and output circuits of ICs a number of diodes are present, some desired and some parasitic. As already shown in the above section, these components represent additional current paths, and as a result of random contacting of the connector, undefined current paths may result. As a result, undefined currents may flow into the component, either via the clamping

diodes to the inputs and outputs, or via additional parasitic diodes in the ICs. In order to avoid uncontrolled operational states, changing subsystems whilst powered up is basically only permissible if the subsystems have a a leading GND pin as reference potential.

If the connection of the GND reference potential is first made when inserting subsystems, and only broken after removing them, then operational state which result when changing subsystems can be limited to the cases mentioned above; the assumption is that parts of the system which have the same reference potential are not supplied with voltage.

The inputs of bipolar logic circuits - this applies also for components in the SN74ABT/BCT series - which are in subsystems to be changed, will be at a high-impedance under all conditions. At this point, no problems need therefore be expected. The totem pole outputs of most TTL circuits are at a low resistance when the supply voltage is switched off, as previously mentioned. As a result, when re-inserting a subsystem the line concerned will be switched to Low, and this may be incorrect. 3-state outputs of bipolar circuits are at a high impedance when the supply voltage is switched off; they can, however, go to a low impedance for a short time during switch on or off, and therefore generate an incorrect logic level, since at low supply voltages the internal circuit does not operate properly. The result of this is that during the change of subsystems short-duration undefined signals may appear at the corresponding outputs, which disturb other systems. This problem can be avoided if circuits from the series SN74ABT/BCT are used: as mentioned above, with these components, the outputs are switched into an inactive, high impedance state, if the supply voltage falls below about 3 V.

Whereas the problem of changing subsystems under voltage can be easily solved, particularly when using components which include a supply-voltage monitor, CMOS circuits can only be used under these circumstances with certain restrictions. In this case too, the use of a leading GND pin on the connector is essential. The CMOS inputs of circuits on the subsystem to be changed should in every case be protected at least with series resistors (see Fig 8a), in order to prevent excessive currents in the clamping diodes of the input protection circuitry. In extreme cases, depending on the layout of pins on the connector, the current for the complete subsystem could for a short time flow through one of these diodes! For the outputs of CMOS circuits, no practicable protection circuit can be recommended. Also the use of protection resistors must be considered, in order to limit the current in the clamping diodes at the output; this is however in most cases not possible, since this would result in an unacceptable reduction in the output drive capability.

3. Unused inputs

In many cases functions, or parts of functions, of digital ICs are unused: for example, when only two inputs of a three input AND gate are used. In no circumstances should such parts be left unconnected, because the undefined voltages at the outside connections will result in undefined operational states. A rule which must be observed under all circumstances is as follows:

> At all unused inputs of digital ICs, defined logic levels (Low or High) must be applied in every case.

The logic level which should be applied to any particular unused input depends on the function of the circuit. As a result of the input circuits of bipolar ICs, a High level will be established at open circuited inputs. If the voltage at such an input is measured, it will be found to correspond to the threshold voltage of the input circuit - about 1.4 V, or 1.1 V with circuits from the family SN74LS. With a test of the function of such circuit, this order of voltage at the input in general indicates that this circuit is "open". The situation is different with CMOS circuits: these components are of such high impedance that the smallest charge on the open input can generate any desired logic level. A slight change of the capacitance at the input of such an unconnected input, which can arise by bringing the hand close to the package, can so change the effective voltage at the input that a High level can change into a Low, or vice versa. In addition it should be noted that, for the reasons mentioned above, unconnected inputs may react to all kinds of coupled-in interference voltages, such that the behavior of the circuit can no longer be predicted.

With gates, the best solution is to connect unused inputs to inputs which are in use. The function of the circuit will be unaffected. This circuit arrangement can be used equally well with AND (NAND) as with OR (NOR) gates - see Fig 9. Here it should be noted that connecting the inputs together increases the capacitive load on the driver stage, and with bipolar circuits also increases the DC current drain.

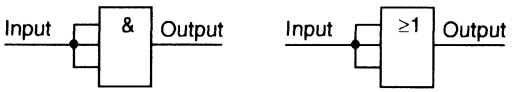

Figure 9: Interconnection of unused inputs with AND and OR gates

In many cases the very simple method shown here can not be used, especially if the unused inputs are not part of complex gate functions. In this case a defined logic level must be applied to the inputs. If a Low level is required, the input should be directly connected to GND; if a High is required, then it should be connected with a voltage source corresponding with a High level. In general this will be the positive supply voltage V_{CC}. Fig 10 shows how in the previously mentioned cases a fixed potential should be connected to unused inputs. It should be noted that a High level should be applied to the unused inputs of an AND(NAND) function, and a Low level to unused inputs of an OR(NOR) function.

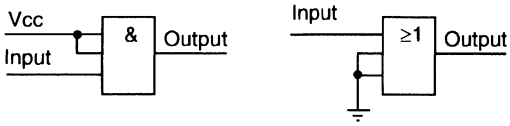

Figure 10: A fixed potential connected to unused inputs

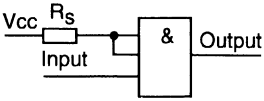

Figure 11: Series resistor connected to unused inputs of multi-emitter transistors

Exception to the above are circuits with multi-emitter inputs (series SN74 and SN74S). Since no voltage greater than 5.5 V should be applied to the inputs of these circuit (because if exceeded, the base-emitter junction at the inputs will break down) the inputs of these circuits must be connected to the supply voltage V_{CC} via a series resistor R_S. This resistor should be dimensioned such that the current flowing into the gate or gates which results from over voltage does not exceed 1 mA. On the other hand, the High level input current of the circuits connected to the gate flows through this resistor. The resistor should therefore be so dimensioned that the voltage drop across it still allows the required High level. This results in the following formulae (1) and (2) for dimensioning the resistor R_S. Several inputs can be connected to a High level via a single resistor, providing the following conditions are met:

$$R_{s\,min} = \frac{V_{ccp} - 5,5V}{1mA} \qquad (1)$$

$$R_{s\,max} = \frac{V_{cc\,min} - 2,4V}{n \cdot I_{ih}} \qquad (2)$$

where
- V_{ccp} = maximum peak voltage of the supply voltage V_{CC} (approx. 7 V)
- V_{ccmin} = minimum supply voltage V_{CC}
- I_{ih} = High input current (typ 40 µA)
- n = number of inputs connected

If whole parts of an integrated circuit are unused, then the rules above should be applied. If for example in an application only one flip-flop from a dual flip-flop type SN74ALS74 is used, then all inputs of the unused flip-flop should be connected to a defined logic level, which in this case could be either Low or High.

Unused outputs of a circuit should basically not be left unconnected.

4. Excessive input currents

All integrated circuits are provided with protection circuits at outside connections, in the form of diodes or similar components, which are intended to protect the circuit against destruction as a result of electrostatic discharge. In addition such circuits are provided with clamping diodes at their inputs, whose job is to limit over- and undervoltage resulting from line reflections, and to divert the currents which flow in consequence to either the negative (GND) or positive (V_{CC}) supply rails. Currents which flow in these circuit parts can, under certain circumstances, activate so-called parasitic transistors, and thereby result in an incorrect operation of the circuit.

An example of this are the clamping diodes at the inputs of HCMOS circuits, which are intended to limit overvoltages resulting from reflections. These diodes are created with a P-doped region in an N-doped substrate, which in turn is connected to the positive supply voltage (Fig 12). Between two adjacent diodes, and in conjunction with the substrate, a parasitic PNP transistor is effectively created. A part of the current in one of the two clamping diodes is not therefore diverted to the V_{CC} rail, but instead flows to an adjacent input. The current gain of this transistor is very small (about 0.01), so that under normal operating conditions no effect can be expected. If however a high positive voltage is applied to the input of a circuit as in Fig 12, which adapts signal voltages with an amplitude of 24 V to HCMOS circuits, then a current will flow into the adjacent input, despite the low current gain of the parasitic transistors. The current in the adjacent input may then be sufficient to generate a false input signal. Destruction of, or damage to the integrated circuit (as a result e.g. of "latch up") need however not be feared.

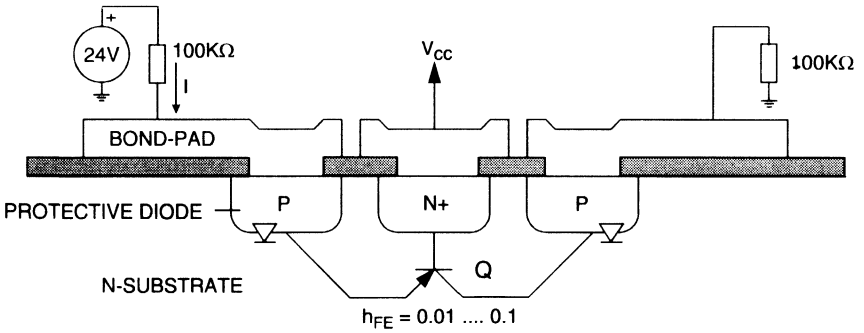

Figure 12: Parasitic transistors in CMOS input stages

Similar effects, which are similarly caused by parasitic transistors, can also be observed with bipolar transistors. Fig 13 shows the input of a logic circuit of this type, which includes the Schottky clamping diodes, realized with an N-doped region covered by a metallic contact. With a small negative input current, the forward voltage of the Schottky diode will be about 400 mV, and the current in such an input will be diverted via the diode to the GND pin of the circuit. If now this current is increased, the forward voltage of the diode will increase accordingly, and at a certain

amplitude will exceed a value of 700 mV. At this point, the silicon diode (which results from the N-doped region and the P-doped substrate under it, connected to the GND of the circuit), will conduct. Here also a parasitic transistor will be activated, whereby the whole adjacent N-doped region, comprising the collectors of active transistors, functions as a collector. This then collects together a part of the current circulating in the substrate. If the amplitude of the negative current is sufficient, incorrect operation of the circuit must again be expected.

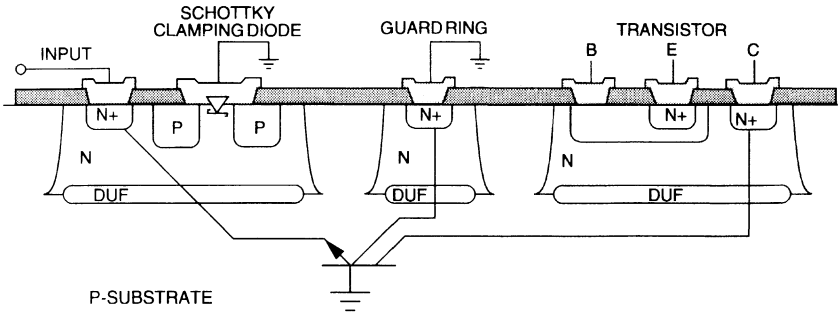

Figure 13: Parasitic transistors in bipolar input circuits

Negative voltage undershoot of considerable amplitude must always be expected in practical operation with logic circuits, and the semiconductor manufacturer must therefore take the steps which are necessary to ensure reliable operation. This is implemented with so-called "guard rings", which are placed in a ring round the circuit in question (Fig 13). In this example these guard rings consist of an N-doped region connected to ground potential, which has the effect of an additional collector for the parasitic transistors, and this collects the majority of the current circulating in the substrate and diverts it to ground potential. These guard rings are so constructed that a negative input current of I_{in} = -60 mA with a duration t = 100 ns does not result in an incorrect function of the circuit. These values are again reflected in the situation represented in Fig 14: here a TTL circuit with a signal amplitude of 3 V drives a 10 m long coaxial cable with a characteristic impedance Z = 50 Ω, at the end of which the input circuitry (with clamping diode) of the circuit in question is connected. Current pulses of high amplitude, such as those generated by line reflection, are catered for with this measuring set-up.

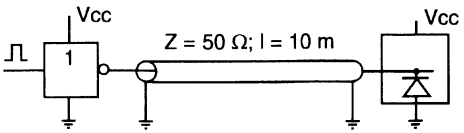

Figure 14: Circuit for generating an undershoot pulse I = -60 mA, t = 100 ns

It should be noted that negative input currents with an amplitude of only a few milliamperes but with a duration of several microseconds can however cause incorrect operation of the circuit. In order not to make the circuit too complicated, when dimensioning the guard rings use is made of the fact that the transit frequency of the parasitic transistors is only about 1 MHz. For this reason a certain duration of the undershoot pulse is necessary in order to switch on the parasitic transistors, and so possibly to cause abnormal operation of the circuit.

5. Transition times

Correct operation of the circuit itself can only be assured if the rise and fall times of the signal at the input do not exceed certain values. With CMOS circuits (SN74HC and 74AC), these values are given in the data sheets. For circuits from the series SN74HC a rise and fall time (transition time) less than 500 ns is specified at V_{CC} = 4.5 V, whilst for ACL circuits (series 74AC) a value of 10 ns/V is given. Fig 15 is intended to explain this in more detail.

The signal amplitude is specified as the difference between the two stable signal levels for High (V_h) and Low (V_l); overshoot and undershoot of the signal are not taken into account. The difference V_h - V_l is taken as 100% of the amplitude. The rise time of the signal is defined as the time taken to rise from 10 % to 90 % of the full amplitude; similarly, the fall time is the time taken to fall from 90 % to 10 % of the amplitude. The pulse width t_w of a signal is measured at 50 % of the amplitude. These definitions must, however, be used for digital circuits with certain qualifications. The reason for this is that in most cases the switching threshold V_t of the input is not 50 % of the amplitude. Because of this, the level needed by the circuit must rather be considered, and from this the required signal waveform be derived.

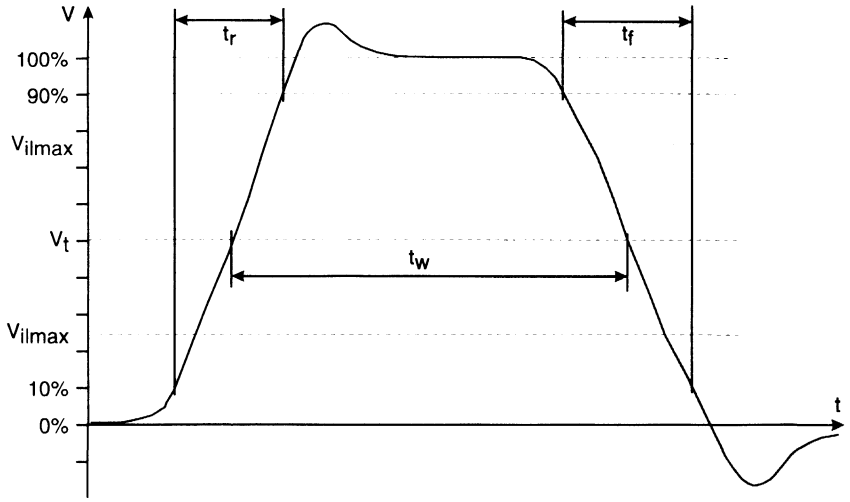

Figure 15: Definition of signal amplitude and pulse width

The values of voltage which are decisive for the correct operation of the circuit are the maximum permissible Low voltage at the input V_{ilmax}, and the minimum necessary High voltage at the input V_{ihmin}. For example, the following applies for a circuit from the series SN74HC:

$$V_{ilmax} = 0.9\ V,\ V_{ihmin} = 3.15\ V\ @\ V_{CC} = 4.5\ V$$

The rise and fall time is however specified between 10 % (0.1 x V_{CC} = 0.45 V) and 90 % (0.9 x V_{CC} = 4.05 V) of the amplitude. The voltage waveform below 0.9 V (Low level) and above 3.15 V (High level) has no influence on the function of the circuit, as long as the absolute maximum ratings are not exceeded. It is therefore better to define rise and fall times over the range between V_{ilmax} and V_{ihmin} which must be adhered to in order to ensure correct functioning of the circuit. From the amplitude (4.5 V) and the rise time specified in the data sheet t_r = 400 ns the transition time rate dt/dv can be derived as follows:

$$dv/dt = \frac{400ns}{0.9 \cdot V_{cc} - 0.1 \cdot V_{cc}} = \frac{400ns}{3.6V} = 110ns/V$$

The input signal must cross the region between V_{ilmax} and V_{ihmin} (and vice versa) at this speed. This value is comparable with the transition rate given in data sheets of the series 74AC of dt/dv = 10 ns/V. The pulse width t_W is measured at the actual threshold voltage V_t of the circuit, and with CMOS circuits at 50 % of the amplitude. Bipolar and TTL-compatible CMOS circuits have a switching threshold which is shifted considerably from the middle of the signal amplitude, which must then be taken into account when determining the pulse width. The following Table 1 shows the necessary transition rise/fall rates for various logic families.

Table 1: Transition rise/fall rates of logic circuits

Series	V_{CC} (V)	Vilmax (V)	Vihmin (V)	Vt (V)	dt/dv (ns/V)
SN74	4.75 - 5.25	0.8	2.0	1.4	100
SN74LS	4.75 - 5.25	0.8	2.0	1.4	50
SN74S	4.75 - 5.25	0.8	2.0	1.4	50
SN74ALS	4.5 - 5.5	0.8	2.0	1.4	15
SN74AS	4.5 - 5.5	0.8	2.0	1.4	8
SN74F	4.5 - 5.5	0.8	2.0	1.4	8
SN74HC	2.0	0.3	1.5	1.4	625
	4.6	0.9	3.15	2.25	110
	6	1.2	4.2	3.0	80
SN74HCT	4.5 - 5.5	0.8	2.0	1.4	125
74AC	3.0	0.9	2.1	1.5	10
	4.5	1.35	3.15	2.25	10
	5.5	1.65	3.85	2.75	10
74ACT	4.5 - 5.5	0.8	2.0	1.4	10
SN74BCT	4.5 - 5.5	0.8	2.0	1.4	10
SN74ABT	4.5 - 5.5	0.8	2.0	1.4	5/10
SN74LV	2.7 - 3.6	0.8	2.0	~ 1.5	100
SN74LVC	2.7 - 3.6	0.8	2.0	~ 1.5	5/10
SN74LVT	3.0 - 3.6	0.8	2.0	1.4	10

The values given here for the transition rise/fall rates dt/dv are to be so understood, that the function of individual components will be ensured if the circuit is controlled with these rates. This does not however necessarily mean that the circuit will operate correctly under all circumstances in a large system. The circuit shown in Fig 16 should explain this in more detail. It shows two D-type flip-flops connected as a two-stage shift register. The first flip-flop is the TTL-compatible circuit 74ACT11074 (input threshold voltage = 1.5V), whereas the second flip-flop 74AC11074 has CMOS-compatible inputs, with an input threshold voltage of 0.5 x V_{CC}.

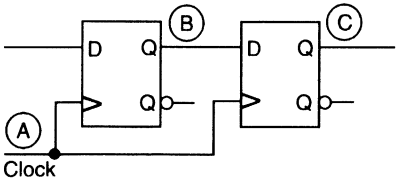

Figure 16: Two-stage shift register

According to Table 1, circuits of the series 74AC(T) must be controlled with a transition rate of at least 10 ns/V, if the function of individual components is to be assured. If however the behavior with time of the circuit is analyzed, it will be found that the shift-register does not behave as required (Fig 17). When the clock signal reaches a level of 1.5 V, having the required transition rate of 10 ns/V, then the first

flip-flop will switch. The output reacts about (this is a typical value!) 5 ns later. Only after another 5 ns does the voltage of the clock signal reach a value of 2.5 V, such that the second flip-flop switches. As a result of this late triggering, it accepts incorrect information: namely, the state that the first flip-flop has reached after the switching clock edge, and not that which the flip-flop had before the clock edge.

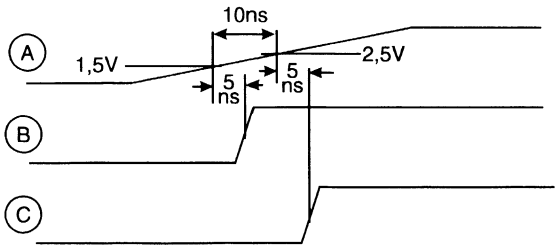

Figure 17: Timing diagram explaining incorrect operation of a shift register

Under typical operating conditions, the circuit would however operate perfectly correctly. The output signals of "Advanced CMOS" circuits have a rise time < 5 ns (typical 2 ns). With the clock signal a voltage change of 1.5 V to 2.5 V takes place in about 1.25 ns. A flip-flop of the type 74AC(T)11074 has a minimum delay time of 1.5 ns, so that under these circumstances correct functioning of the circuit is assured.

In the same way problems need not be expected when using circuits from other families under similar conditions, as long as the signals have their nominal rise and fall times. Under extreme conditions (for example, with unfavorable line routing) the switching times can however be so lengthened that faults of the kind described above may occur.

6. Propagation delay times

6.1. Propagation delay times with several outputs switching simultaneously

The propagation delay times of circuits given in data sheets apply when only one output switches at a time. The reason for this is that the equipment used to test circuits is able only to test one transmission channel at a time. If several outputs switch simultaneously, the propagation delay times given in data sheets can only be used with reservations. The reason for this is that the package inductances L_p of the supply voltage lines as well the output lines (see Fig 18) have a significant influence on the circuits, and thus on the delay times. These inductances have the effect that the current in the power supply lines, and consequently in the output of the circuit, has a limited rate of rise. For this reason, when several outputs switch simultaneously, only a limited output current is available.

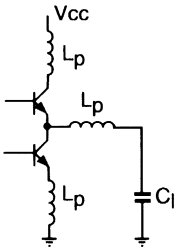

Figure 18: Inductances in the lines supplying a package

Fig 19 shows the influence on the delay time of the number of outputs which are switched simultaneously. When packages having two supply voltage pins (V_{CC} and GND) are used, as is the case with the majority of digital integrated circuits, an increase of the delay time of 150 - 200 ps for each additional output which is simultaneously switched must be expected. With an octal bus driver such as the SN74xx240, the delay time is thus increased by 1 - 1.4 ns when all eight outputs switch simultaneously. In those cases where there are several supply voltage pins, such as the "Advanced CMOS" circuits in the series 74ACT from Texas Instruments, the result is consequently an influence on the speed of the circuit. As can be seen in Fig 19, the loss of speed of the components is then halved, when several outputs switch simultaneously.

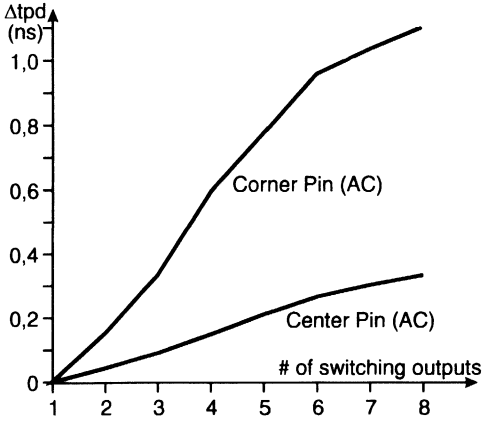

Figure 19: Increase of the delay time when several outputs are switched simultaneously

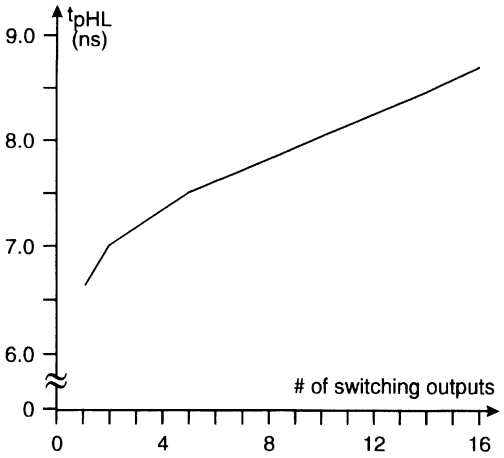

Figure 20: Increase of the propagation delay time with Widebus circuits SN74AC16240

With bus drivers and also VLSI circuits, which have more than eight outputs which switch simultaneously, an appropriate number of additional supply voltage pins are therefore provided. A good example is given by the "Widebus" circuits from Texas Instruments, which are bus drivers with 16, 18 or 20 channels. In order to keep the loss of speed with so many outputs within limits, with these circuits about 25 % of all pins are reserved for the provision of supply voltage. Fig 20 shows the increase of the delay time of a 74AC16240 as a function of the number of outputs which are switched simultaneously.

6.2. Propagation delay times with negative undershooting at the outputs

With bipolar circuits, negative voltages which are caused by undershooting can influence the function of the component. Fig 21 shows a circuit which will be used to describe this effect. This circuit represents the output stage of a bus driver, which should be in an inactive and high-resistance state. Another, this time active, bus driver U_1 switches the line between the two circuits from a High to a Low level. As a result of a typically inadequate termination of the line, there is a negative undershoot on the line, which cause a current I_x to flow in the internal circuit of the output stage; this current flows via the collector-base diode of the transistor Q5 and the Schottky diode D_1 in parallel with it. This current flows further via the transistor Q1, to the base node of transistor Q2. Now this node is clamped to a Low level. If this output stage should again be switched into the active state (OUTPUT ENABLE switches from Low High), the output does not follow until the capacitance of the bus line is charged up via the resistor R so far, that the collector base diode of transistor Q_5 is turned off again. This takes typically 5 to 10 ns. Apparently the delay time to again switch on the output stage is increased by about this amount.

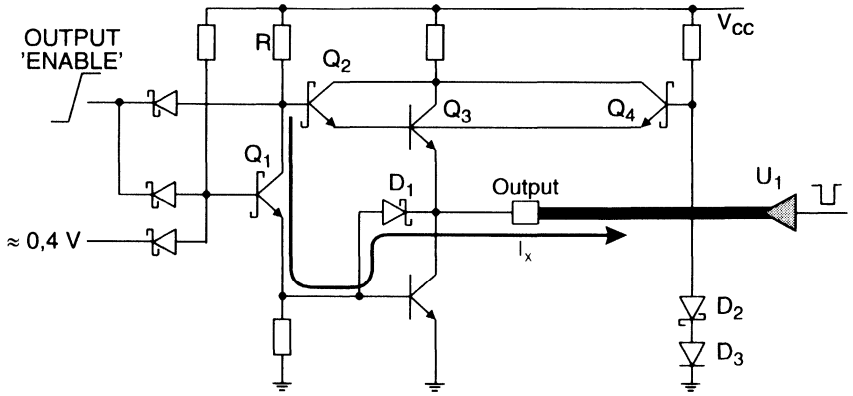

Figure 21: Currents in the output stage of a bus driver with negative undershoot

In order to prevent this effect, a clamping circuit (D_2, D_3, Q_4 in Fig 21) is integrated into modern bus drivers. This ensures that, should the output voltage go below -0.3 V, the transistor Q_3 switches on the output stage, and therefore that the current I_x is diverted to the positive supply voltage rail V_{CC}. With ABT circuits this is unnecessary. In these circuits a completely different circuit is used, where the phenomenon described here can no more become effective.

6.3. Propagation delay times with large capacitive loads

In data sheets of digital integrated circuits, the propagation delay times are specified with a capacitive load of 50 pF (or 15 pF, on older logic families). This value represents the capacitive load with which the test circuit loads the output of the IC while it is being tested. This value is also the capacitive load when the output drives about five inputs of other circuits; this assumes that the length of the connecting lines is only a few centimeters, as is typically the case on printed circuit boards. With such short lines, the simplified assumption is made that the line itself behaves like a capacitor, which additionally loads the output and influences the propagation delay time accordingly. However, with long lines this assumption leads to errors, because the signal delay is actually determined by the propagation speed of the electrical wave front along the line. In fact the propagation delay time of the integrated circuit itself is determined by the loading of the output, that is, by the characteristic impedance of line to which it is connected, and not from its length or capacitance. Fig 23 shows the waveform at the output of a circuit type SN74LS00, which is driving a line terminated at its end with a resistance of 100 Ω, and has a length of 0 m (resistor connected directly to the output), 1 m and 11 m - see Fig 22. The three resulting output signals are shown staggered, and will be seen to be practically identical: i.e. the propagation delay time of the integrated circuit is not influenced. The length of the line, and the resulting signal propagation time (5 ns/m), do however indeed have an influence on the delay time of the complete system. The propagation time of the wave along a 11 m long transmission line results then in 55 ns. Adding

the propagation delay time of the SN74LS00 of about 10 ns leads to a total delay of 65 ns.

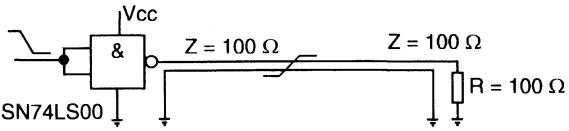

Figure 22: Measurement circuit

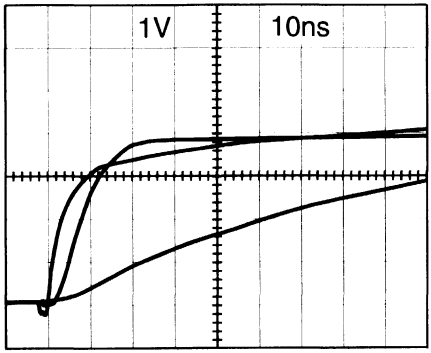

Figure 23: Waveforms with various line lengths

If the capacitive load connected to the output of a circuit is represented as a single capacitor, the resulting propagation delay time can be relatively simply calculated. A purely capacitive load can for example be assumed, if the output of the integrated circuit controls an MOS power transistor with an relatively large input capacitance. To a first approximation this assumption is correct if, as mentioned above, an output drives adjacent inputs over a line with a length of only a few centimeters. The propagation delay times given in data sheets comprehend the following:

- The propagation delay time through the internal circuitry of the IC,
- the delay resulting from the switching time of the output stage,
- and lastly the time needed to charge and discharge the capacitance of the test circuit, typically 50 pF.

Whereas the first two parts are independent of the load which is connected, the last part must take account of the actual load, whereby a load capacitance C_1 = 50 pF (15 pF) is already given in data sheets. The time taken to charge the additional capacitance is determined by the current which the circuit is able to deliver. For the High level, this value can be deduced indirectly from the data sheet. Fig 24 shows the relevant part of the circuit of a bipolar output stage, together with the resulting output characteristics.

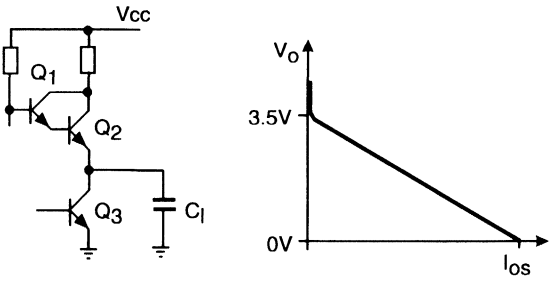

Figure 24: Bipolar output stage with output characteristics at a High level

The short circuit current of the output when at a High level is determined by the resistance R_1, together with the saturation voltage of the Darlington transistors Q_1 and Q_2, together with their collector path resistance. The internal resistance R_O of a circuit can be determined with sufficient accuracy from the open circuit output voltage (typically 3.5 V), together with the short circuit current I_{OS} given in the data sheet, using the following formula (3):

$$R_o = \frac{3.5V}{I_{os}} \qquad (3)$$

With circuits which use MOS transistors in their output stages (SN74HC and 74AC), the output current is decided by the size of the transistors and the potential difference between gate and source. Since there is no linear relationship between this voltage and the output current, only an approximate indication of the output resistance can be made.

Table 2 shows the short circuit current I_{OS}, and the internal resistance R_O which results, for the most important circuit types.

The typical output voltage of a bipolar circuit at a Low level is about V_{OI} = 0.3 V. The increase of the delay time resulting from the capacitive load C_I is determined by the time until the external load capacitance has been charged by a voltage source with a voltage V_{Oh} and an internal resistance R_O, from the voltage V_{OI} to the threshold voltage of the circuit of typically V_S = 1.5 V. In this way the delay time t_p resulting from the load capacitance can be calculated from formula (4).

$$\begin{aligned} t_p &= \ln\left(\frac{V_{oh} - V_{ol}}{V_{oh} - V_s}\right) \cdot R_0 \cdot C_l \\ &= \ln\left(\frac{3.5V - 0.3V}{3.5V - 1.5V}\right) \cdot R_o \cdot C_l = 0.5 \cdot R_o \cdot C_l \end{aligned} \qquad (4)$$

Fig 25 shows the waveform of the positive edge at the output of a gate (SN74LS00) with various values of capacitive loads (C_I = 10 pF, 100 pF and 620 pF). As expected, the rise time at the output, and the resulting increase of the propagation delay time, are determined by the time constant R_O x C_I.

Table 2: Short circuit current and internal resistance of logic families

Type	Short circuit current I_{OS} (mA)	Internal resistance R_O (Ω)
SN7400	35	50
SN7440	45	75
SN74LS00	35	100
SN74LS40	65	53
SN74LS240	70	50
SN74S00	65	53
SN74S40	140	25
SN74S240	60	58
SN74ALS00	50	70
SN74ALS40	60	58
SN74ALS240	100	35
SN74ALS1000	120	29
SN74AS00	100	35
SN74AS240	140	24
SN74AS1000	160	21
SN74F00	85	41
SN74F40	140	25
SN74F240	140	25
SN74BCT240	140	25
SN74BCT25240	700	5
SN74ABT240	120	29
SN74HC(T)00	60	40 ... 120
SN74HC(T)240	80	30 ... 100
74AC(T)11000	220	4 ... 25
74AC(T)11240	220	4 ... 25
SN74LV00	35	35 ... 100
SN74LV240	55	25 ... 80
SN74LVC00	85	16 ... 40
SN74LVC240	85	16 ... 40
SN74LVT240	400	8

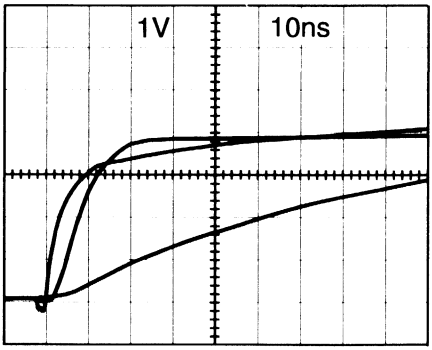

Figure 25: Waveform at the output of a SN74LS00, with C_l = 10 pF, 100 pF and 620 pF

The values needed for the Low level of a bipolar circuit can not be taken directly from data sheets. The transistor Q_3 in Fig 24 is responsible for the output current I_{ol}. As with all semiconductor components, this parameter is non-linear, and in addition is influenced to a large extent by the distribution of components in the circuit on such parameters as current gain, conductance and resistance values etc. For this reason it is possible to make only a rough calculation of the actual output current at Low level. As a first approximation it can be said that the internal resistance of the circuit at Low level is lower than at High level. From this it also follows that in the worst case the increase of the delay time of the negative edge is always smaller than with the positive edge (see Formula 4). The precise value must be determined in individual cases by measurement.

6.4. Input and output capacitances of digital circuits

All digital circuits load capacitively the outputs of the circuits driving them. The input and output capacitances are given in Table 3. These are to be understood as average values, which are typical for the logic family in question. Very different circuit configurations are used within a family, depending on the function and application. For this reason, wide variations from the values given can occur with individual components. In specific cases for new families the values given in data sheets should be taken as a basis. If this data is not available - for example, with older families - the user must make appropriate measurements, if in particular cases more precise values are needed.

The capacitances given in Table 3 were measured at the following voltages:

Bipolar circuits:	V = 2.5V
CMOS circuits:	V = 0 V and V = 2.5V

Table 3: Capacitances of digital circuits

		Output capacitance (pF)	
Series	Input capacitance (pF)	open collector output *)	Bus driver
SN74	3.0	5.0	-
SN74LS	3.5	3.5	5.0
SN74S	3.5	3.5	9.0
SN74ALS	2.0	4.0	5.0
SN74AS	4.0	-	10.0
SN74F	5.0	5.0	9.0
SN74HC	3.0	3.0	9.0
74AC	4.0	-	10.0
SN74BCT	6.0	-	12.0
SN74ABT	4.0	-	8.0
SN74LV	3.0	-	8.0
SN74LVC	4.0	-	8.0
SN74LVT	4.0	-	8.0

*) open collector output of gates and other circuits with low drive capability e.g. SN74xx03. Outputs of bus drivers with open collector have the same output capacitance as totem-pole (3-state) outputs.

7. Bus Conflicts

If several bus drivers with 3-state outputs are connected to a single bus, it can often not be guaranteed under all circumstances that, during the time when switching from one bus driver to another, both will not be active simultaneously for a short time . This results in a short circuit of the outputs and, as a result, in an overload of the circuit. This situation is known as a "bus conflict".

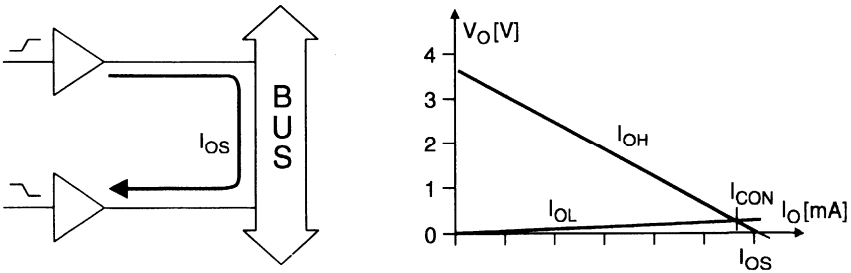

Figure 26: Determining the short circuit current with a bus conflict

The currents which flow as a result can very easily be calculated by means of the output characteristics of the circuits (see also Table 2). As can be seen in Fig 26, the

short circuit current I_{OS} is limited by the High output current of the circuits involved in the "conflict". With bus drivers having an output current I_{OL} = 64 mA (SN74AS, SN74F, SN74BCT or SN74ABT), a current I_{OS} = 120 mA flows in such a case. The power dissipation P_{conl} of the output supplying the Low level can be neglected:

$$P_{conl} = V_{ol} \cdot I_{os} = 0.5V \cdot 120mA = 60mW$$

Even if all eight outputs of a bus driver are involved in such a bus conflict, the total power dissipation will be less than 500 mW. However the situation is different at the outputs supplying the High level. In this case the short circuit power dissipation P_{conh} of each output is as follows:

$$P_{conh} = (V_{cc} - V_{oh}) \cdot I_{os} = 4.5V \cdot 120mA = 0.54W$$

If all eight outputs of a bus driver are involved in this bus conflict the total power dissipation will be about 5 W. When talking about Widebus circuits, it will be 10 W and more.

To analyze the situation inside an integrated circuit under these extreme conditions one has to know, that the heat caused by this power dissipation is not spread over the total chip immediately. Instead one has to consider a certain propagation speed of the heat, which is in the order of 1 µm/µs. That means that during a bus conflict with a duration of a few nanoseconds only, the heat will not be distributed all over the chip. In the first moment the affected component inside the integrated circuit - the transistor or resistor - will be heated up. The resulting increase in temperature can be calculated when knowing the volume of the component in question and the thermal capacitance of silicon. By using the output stage of an ABT circuit (figure 27), this shall be explained in detail. Also, all voltages are shown in this circuit diagram which apply when the output - which should provide a High level - is forced to an output voltage of 0.5 V externally.

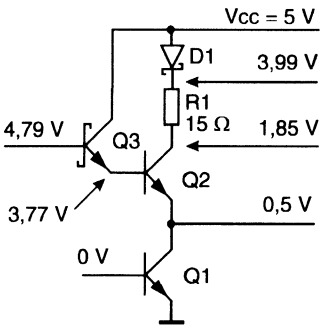

Figure 27: Circuit diagram of an ABT output stage

Table 4 shows the situation in this output stage during a bus conflict. When calculating the volume of the single components, only that volume was considered which is related to the function of this component. For a transistor for example, its

total area was taken into account, but the junction width only - where the heat is dissipated - was considered as the component's height.

Table 4: Situation in an output stage during a bus conflict

	Voltage V (V)	Current I (mA)	Power dissipation P (W)	Volume V (μm^3)	Power dissipation /volume ($W/\mu m^3$)
D_1	1.01	142	0.156	3200	46×10^{-6}
R_1	2.14	142	0.304	3840	79×10^{-6}
Q_2	1.35	142	0.192	495	38×10^{-3}

According to this analysis the highest power dissipation per volume unit is found in transistor Q_2. This is caused by the fact that the junction width of 0.5 µm only was considered as height of this component. By using the formula (5), one can now calculate the temperature increase, $\Delta\vartheta$:

$$\Delta\vartheta = \frac{P \cdot t}{V \cdot c_p} \qquad (5)$$

with P = power dissipation
V = volume
t = time
c_P = heat capacitance of silicon = 1,631 x 10^{-3} Ws / Kmm^3

Considering a propagation speed of the heat of 1 µm/µs and a junction width of 0.5 µm, one can assume that during the first 500 ns of a bus conflict the heat will not be distributed over the chip, but will stay in the transistor junction. Under this condition the temperature increase $\Delta\vartheta$ will be as follows:

$$\Delta\vartheta = \frac{0{,}192W \cdot 500ns}{495\mu m^3 \cdot 1{,}631 \cdot 10^{-3} \frac{W \cdot s}{K \cdot mm^3}} = 119K$$

Short bus conflicts with a duration of a few or few tens nanoseconds will cause a temperature increase of the component in question of some ten degrees only. Therefore a degradation of the reliability of the component is unlikely. Furthermore one can assume that in well designed systems the period of bus conflicts will be high compared to the duration of the bus conflict (period : duration > 10 : 1). To be on the safe side, the mean chip temperature should be calculated in any case, to be sure that this temperature does not increase beyond 150 °C. Beyond this temperature the thermal expansion coefficient of the plastic material of the package becomes very different from the expansion coefficient of silicon. This fact is likely to lead to a mechanical stress at high temperatures, which may result in a flaw of the bond wire.

The total power dissipation P_{tot} of a bus driver is calculated by the following formula (6):

$$P_{tot} = P_0 + (P_s \cdot t_s + P_c \cdot 2 \cdot \tau + P_{con} \cdot t_{con}) \cdot f \cdot n \quad (6)$$

with
- P_O = quiescent power dissipation
- P_S = power dissipation resulting from current spikes when output switch
- t_S = duration of current spike
- P_C = power dissipation when (dis)charging the bus capacitance
- τ = signal propagation time on the bus
- P_{con} = power dissipation during bus conflict
- t_{con} = duration of bus conflict
- f = frequency
- n = number of outputs at which a bus conflict occurs

The power dissipation of a bus driver will now be calculated in a practical example. In this case, the following assumptions have been made:

Circuit: SN74F245
P_O = 0.45 W (from data sheet)
P_S = 5V x 30 mA = 0.15 mW with t_S = 5 ns (measured)

To calculate the power dissipation P_C that occurs when charging the capacitance of the bus line, the voltage waveform at the output and with the given load (the line impedance) must be known. The easiest way to determine this is to make use of the Bergeron diagram. With a line impedance of 30 Ω the result then is that a stable state is reached after double the signal propagation time with a positive edge. That is to say, for this time a current is supplied into the line from the driver circuit. The amplitude of the preceding waveform, and therefore of the output voltage of the circuit, is about V_O = 2V. The power dissipation during this time and under these load conditions can then be calculated as follows:

$$\begin{aligned} P_c &= (V_{cc} - V_o) \cdot V_o / Z_o \\ &= (5V - 2V) \cdot 2V / 30\Omega = 0.2W \end{aligned} \quad (7)$$

The signal propagation time on a backplane in a 19-inch rack (wire length about 40 cm) is τ = 10 ns.

If further assuming a bus cycle time is 100 ns (f = 10 MHz), a duration of the bus conflict of 10 ns, and that all eight outputs of the circuit are involved, then the resulting total power dissipation is as follows:

$$\begin{aligned} P_{tot} &= 0.45W + (0.15W \cdot 5ns + 0.2W \cdot 2 \cdot 10ns + 0.53W \cdot 10ns) \cdot 10MHz \cdot 8 \\ &= 0.45W + (0,75nWs + 4nWs + 5.3nWs) \cdot 10MHz \cdot 8 \\ &= 1.29W \end{aligned}$$

This power dissipation results in a rise of temperature of the silicon chip, which in turn influences the reliability of the circuit. The chip temperature can be calculated as follows:

$$T_j = T_a + P_{tot} \cdot R_{\vartheta ja} \qquad (8)$$

with T_j = chip temperature
T_a = ambient temperature
$R_{\vartheta ja}$ = thermal resistance of package

Table 5 shows the typical thermal resistance of the packages which are mostly used for digital circuits. These must be considered as typical values, because a number of factors determine the actual value, including chip the size, the lead-frame material, the composition of the plastic, the ambient air flow, and the thermal properties of the circuit board. The values given apply if the circuit is soldered onto a PCB.

Table 5: Thermal resistance of plastic packages in still air

	Thermal resistance (°C/W)	
Number of pins	DIL package	SO package
14	86	117
16	80	110
20	78	95
24	73	85

According to the above table, the thermal resistance of a 20-pin DIL package is $R_{\vartheta ja}$ = 78 °C/W. This means that, in the example given above, the chip temperature would be about 100 degrees above the ambient temperature. The chip temperature must not be allowed to exceed 150 °C, because otherwise the reliability would be much reduced as a result of the causes mentioned above. Therefore the maximum permissible ambient temperature is in this case 150 °C - 100 °C = 50 °C.

In cases where bus conflict may occur - and that is the situation with practically all bus applications - power dissipation is therefore of particular importance. There is usually nothing that can be done about dynamic conditions (the frequency of operation) without adversely affecting the performance of the system with respect to data rate. Also, the overlap of operating states can not always be prevented if worst-case conditions are taken into account. However it can be said that bus conflicts of a duration of a few or a few ten nanoseconds should not be a problem. The choice of the most suitable components allows control of the quiescent power dissipation. With fast bipolar logic families (SN74S, SN74AS and SN74F) the permissible total power dissipation might very soon be exceeded because of their high quiescent power dissipation. Better in this respect are the series SN74LS and SN74ALS: because of their considerably lower quiescent current requirements, bus conflicts do not result in over-dissipation in most cases. Even better are circuits from the BiCMOS series, SN74BCT and SN74ABT, and of course all CMOS circuits, although with the latter

ones a part of the advantage of their low quiescent current is lost again by a higher dynamic power dissipation.

One application area however became very critical today: bus conflicts during the power-on phase of a system. These bus conflicts are caused by the fact that during the power-on phase (system reset) the supervising circuit does not provide defined control signals, while the rest of the system may already be functional. Therefore there is a high probability that various bus drivers may be activated accidentally at the same time. This again results in bus conflicts which may last several 100 ms (duration of the power-on phase or reset time). Now one has to know that the thermal time constant of an integrated circuit is about 1 to 5 ms only. That means that after this time one has to expect the final temperature in the device caused by momentary power dissipation. If again - as calculated above - a total power dissipation of 5 W in an 8-bit device during this bus conflict situation is assumed, a theoretical over-temperature of the chip of 500 °C has to be considered. With Widebus-Circuits the theoretical over-temperature will be 1000 °C. These components are mostly immediately destroyed during the kind of bus conflicts discussed here. Even if with other circuits no defect is detected after such a bus conflict directly, in any case a dramatic degradation of the device has to be expected, which after some operation time or some further bus conflicts leads to a final destruction of the component.

To avoid bus conflicts during the power-on phase of a system, additional effort is required. At first, the designer should make sure, that an adequate design of the control logic prevents these bus conflicts. Very often that is not quite easy, due to the reason that during the power-on phase one can not expect a defined supply voltage and therefore also no defined operation of the logic circuits. The supply voltage range below 3 V is mostly not critical. Many advanced bus drivers already contain a supply voltage monitor which disables the outputs (3-state) as long as the supply voltage is lower than about 3 V. Furthermore below this voltage an overload of the components is unlikely, due to the reason that under this condition the drive capability is very limited. Beyond a supply voltage of 3 V additional measures are necessary. One method is to connect a pull-up resistor between the enable inputs of the bus interface circuits in question and the positive supply rail, which may ensure a high level as long as the preceding control logic does not provide a defined logic level. This measure however will not be helpful if the mentioned control logic delivers a defined but wrong logic level. A much more complex but also always reliable solution to the problem is to disable all bus interface circuits in question during the critical time by additional control logic (Fig 28). In this circuit a supply voltage monitor TLC7705 provides a signal which disables all bus drivers during the critical time period, and may also reset the main processor and by this the control logic of the system. Advantageous for this kind of applications are bus interface circuits which provide two enable inputs like the SN74ABT541: one control input is connected - as in the past - to control the normal operation by the system control logic, while the other input is connected to the monitor device to disable the bus logic whenever an undefined system condition - e.g. during power-on - is expected. If no second enable input is available - like in a SN74ABT245 - an further gate is required to perform the additional disable function.

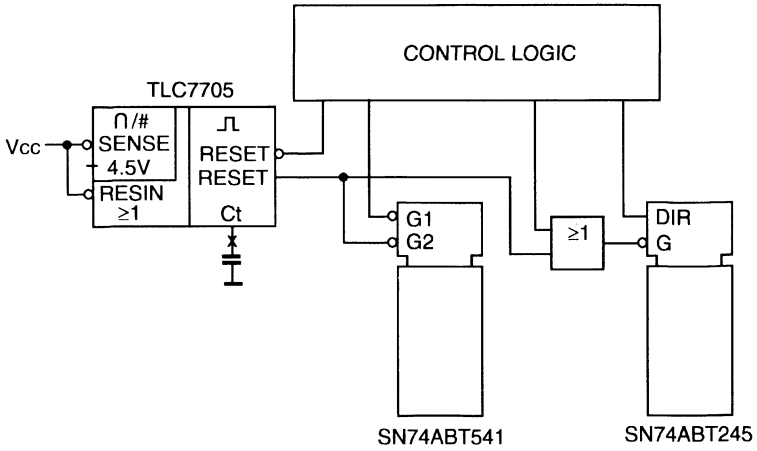

Figure 28: Bus supervision during power-on

WARNING

Since during bus conflicts on signal lines currents will flow which are considerably higher than with normal operation, the noise margin in the system is reduced accordingly. This can result in faulty operation. For this reason alone, care should therefore be taken to avoid bus conflicts.

8. Backdriving

The testing of highly complex electronic systems has always been a problem since they were first developed; such testing must ensure that the system or subsystem operates faultlessly. For this purpose it is of advantage to install diagnostic programs at system level, which are able to recognize faults, and preferably also to localize them. Certain limitations are unavoidable with self testing, since a defective system may often no longer be able to seek and localize faults. This method usually breaks down completely when attempting to test individual component groups, since their "intelligence" - that is to say, their ability to conduct fault diagnosis on their own - is generally too limited. In such cases additional test equipment is necessary which stimulates the component group with special test signals (test samples or patterns) and analyzes the results.

If the component group is conceived such that all relevant circuit segments can be addressed via a defined interface ("Built In Testability" = BIT), then such testing can be performed without the need for much in the way of additional test circuits and adapters. A good example of this is the test bus IEEE1149.1 (JTAG), with which the use of integrated circuits having an appropriate interface allows the test not only of

all circuits themselves, but also of the connections between them, and lastly of the complete subsystem.

If this option is not available, then an attempt must be made, with appropriate signals injected into the circuit from outside, to achieve the required circuit stimulation. For this, the inputs of the circuits or circuit groups which are to be tested must be supplied with the necessary voltages (with digital circuits, with e.g. logic Low or High) via nail-bed adapters. The reaction at the outputs of these circuits is now monitored. In this way the function even of complex systems can be tested step by step, and the most common faults recognized:

- Solder bridges, and broken metallisation
- Incorrect, faulty, damaged or missing components
- Functional disturbances and signal processing faults

Since only a few single components are addressed at a time, this method has the advantage that only the special, appropriate functions (e.g. the truth table of a gate) need to be known, and not the function of the complete component group. In this way, standard test program libraries for the circuits in question can be used to put together the complete test program. With this method, large systems can also be tested step by step, without having to make use of excessively complex test procedures.
The stimulation of the circuit or circuit group which is to be tested may present a problem. As mentioned above, the inputs of, for example the gate G_3 in Fig 29 must be switched to a particular potential. These same inputs will however be already controlled by other circuits (G_1 and G_2), which themselves supply their own signals to the gates to be tested. The test equipment must therefore be able to force another voltage on to the node point in the circuit as that supplied by the existing circuit. The expression commonly used here is of "**backdriving**" or "node forcing": the output of a circuit is forced from outside into another state to that corresponding to its normal control logic.

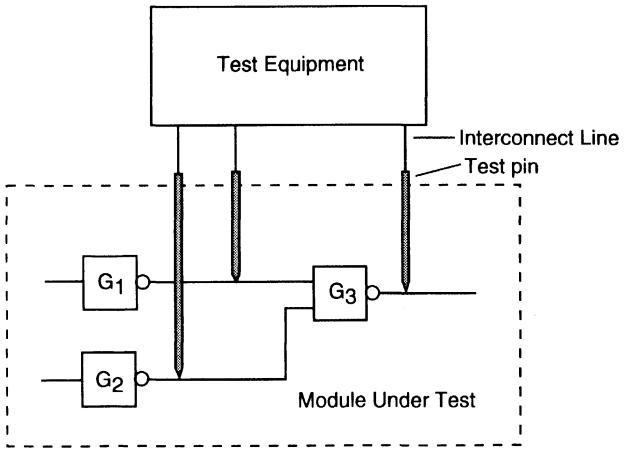

Figure 29: Feeding test signals into a node test point

Since the output of an integrated circuit can deliver a comparatively high current, the test equipment must have substantial drive capability, in order to be able to force the circuit from outside into another logic state. Table 2 gives the short-circuit current at High level of the most important logic families. However, even the situation in which the test equipment must force an output to Low level is not the most demanding requirement. Currents up to several 100 mA must be provided, in order to force from outside an output which is supplying a Low level, into a High level state.

A basic problem is the serious interference which inevitably arises when the high currents mentioned above are switched on or off. In addition, in these circumstances line reflections occur on the lines connecting the test equipment and the circuit being tested. All these effects can result in a malfunction (either real or apparent) of the circuit being tested. This test method is therefore of only limited application when the precise timing of fast circuits must be assessed.

A further serious problem is that, when injecting the test signal current into the outputs, which must then be forced into an inverted state, the circuits will mostly be driven far outside their maximum permissible ratings. This results in the danger of damage to, or even destruction of the circuits; at the very least their reliability and therefore their operating life will be adversely affected. An additional factor is that in recent years the drive capability - that is, the maximum output currents - of integrated circuits has been steadily increased, in the interest of improved technical performance. Whereas the introduction of this testing concept twenty years ago would have required test equipment to deliver currents of only up to 100 mA, in order to force the outputs of circuits available at that time to particular logic levels, with modern bus drivers currents of 500 mA and more are needed (see Figure 30).
The high current densities in the internal connections of the integrated circuit which result from this can cause a drift of metallic ions, or so-called electromigration. This effect begins at current densities of $3 \times 10^5 \cdots 10^6$ A/cm^2. The result is that metallic ions are released from the grain boundaries, which then drift in the invers direction of

current flow (that means in the direction of the electron flow). In this manner, if the excessive current density lasts long enough, the interconnections will be eroded.

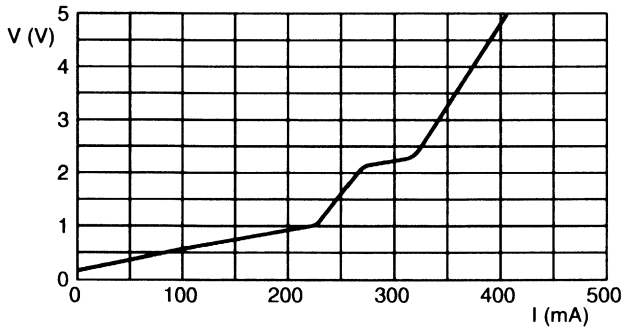

Figure 30: Low output characteristic of a SN74AS645

When Backdriving, the most important effect is, however, the extreme rise of temperature which occurs in the silicon chip during the test. The heat which results from this must be conducted away via the package. The equivalent circuit of Figure 31 is intended to describe the thermal relationships in the package.

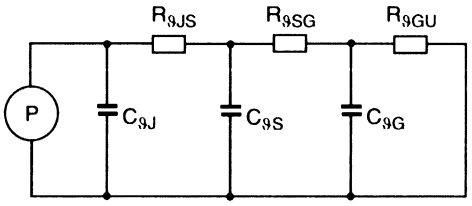

Figure 31: Thermal resistances in an integrated circuit

P	= Thermal Source
$C_{\vartheta J}$	= Thermal Capacitance of the Junction
$C_{\vartheta S}$	= Thermal Capacitance of the Substrate
$C_{\vartheta G}$	= Thermal Capacitance of the Package
$R_{\vartheta JS}$	= Thermal Resistance Junction-Substrate
$R_{\vartheta SG}$	= Thermal Resistance Substrate-Package
$R_{\vartheta GU}$	= Thermal Resistance Package-Ambient

The Thermal Source P first fills up the thermal capacitance of the semiconductor junction. The heat spreads via the thermal resistance $R_{\vartheta JS}$ in the complete substrate (chip) of the integrated circuit. From there the heat flows via the resistance $R_{\vartheta SG}$ into the package, and then via the resistance $R_{\vartheta GU}$ to the ambient environment. Only the sum of the thermal resistances $R_{\vartheta JU} = R_{\vartheta JS} + R_{\vartheta SG} + R_{\vartheta GU}$ (Thermal Resistance Junction-Ambient) is given in Data Books (see also Table 5). This resistance is however not of help for the problem under consideration. It is true that it can be used to calculate the temperature in a stable state. Rapid temperature rises,

such as result from the heavy loads of short duration which arise with Backdriving, can not however be calculated from the sum of thermal resistances. The thermal capacitance and also the thermal conductivity of the silicon chip can be calculated in a simplified fashion. The corresponding figures for the package are not however readily available. It is therefore better to determine the thermal behavior in an integrated circuit by means of measurements (see Figure 32).

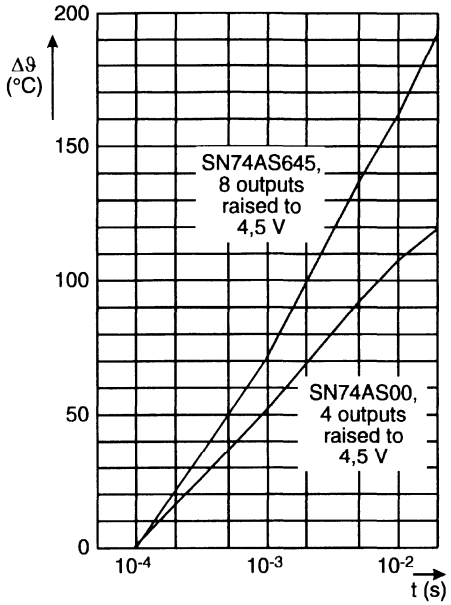

Figure 32: Thermal behavior in an integrated circuit

From this it can be seen that, with a SN74AS645, a temperature rise of the chip of 100 °C must be expected after 2 ms; after 10 ms temperatures will even be attained which are no longer permissible in plastic packages. CMOS and BiCMOS circuits, which are distinguished in applications by a very low power dissipation, do not behave any better in this particular case. With these modern components one must expect at least the same driving capability. The short-circuit current at the output of an ACL Integrated Circuit is > 250 mA); and it is ultimately these currents which are responsible for the high power dissipation during Backdriving.

For the above reasons, the following rules should always be observed when using these test methods:

1. "Backdriving" should only be used when absolutely necessary. It should be used only where the state required at the node point in question can be reached in no other way.

2. The maximum permissible power dissipation of an integrated circuit should in no circumstances be exceeded.
3. Outputs which are at a Low level state as a result of their logic functions may be raised to a level of V_O = 3 V for a short period by means of "Backdriving". The energy which, as a result of this, is injected into the circuit (V_O x I_{OI} x t_d) must not exceed 25 mWs. The current which results in an output should not exceed a value of I_{OI} = 300 mA. The pulse duration must not exceed t_d = 100 ms. In order to keep the thermal stress within acceptable limits, the duty cycle of the pulses (duration of the pulse / duration of the period) should be less than 1 : 10.
4. Outputs which are in a High level state as a result of their logic functions may be lowered to a level of 0 V for a short time by means of "Backdriving". One output of a circuit may be short circuited to ground in such a case for maximum t_d = 100 ms. The product of the output current, the supply voltage and the pulse duration (I_{OH} x V_{CC} x t_d) must again not exceed 25 mWs. If n outputs are simultaneously short-circuited to ground, care must be taken to limit the total energy injected into the device under test (I_{OH} x V_{CC} x t_d) to 25 mWs. In order to keep the thermal stress within reasonable limits, the duty cycle of the short circuit (short circuit duration / repetition time) should be less than 1 : 10.
5. All voltages, including peak voltages of overshoots / undershoots, must be within the absolute maximum ratings on data sheets.
6. Simultaneous "Backdriving" of several outputs in parallel (wired OR) with a common current source is not permissible. Since current sharing can not be predicted, there is otherwise danger of overloading the circuit.
7. The chip temperature of the circuit under test must not exceed 125 °C.
8. Open-circuit (unterminated) lines should be avoided, in order to prevent faults caused by reflection.

It should be mentioned that semiconductor component manufacturers see testing with "Backdriving" as involving a measure of risk. The danger of overloading components can not be excluded, since they are thereby operated in regions which may lie far outside those for which they were designed. For this reason, no statement about the reliability of components which are subjected to this test procedure can be made. Texas Instruments itself does not make use of such test methods, the more so because they are not permissible in many (e.g. military) areas of application.

9. Conclusion

This report should have provided the designer of digital systems with a wealth of information which is not to be found in data books, but which is of interest and necessary in very many applications. The differences between individual circuit families has been highlighted. The circuit design techniques which are used with various components, combined with the different technologies which are used to manufacture them, often make it difficult to give specific design rules; in many cases it is only possible to give very general guidance. One reason for this is that few parameters are actually measured, particularly with older components. In all such cases, this report should at least have provided "rules of thumb" which enable the designer to predict the behavior of the circuits in his system.

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